In some examples, the counters **704***a*, **704***b* can be internal counters in the controller **702**. The controller **702** receives one or more input tuning signals and controls the PWM generator **707** to adjust the effective capacitance of the capacitors **302***a*, **302***b* based on the input tuning signal(s).

**[0081]** The PWM generator **707** generates PWM signals used to control the switches **304***a*, **304***b*. The ON timing, or ZVS timing, of the switches **304***a*, **304***b* is controlled by the phase of the PWM signals and the OFF timing, or $T_{ON}$, is controlled by the duty cycle of the PWM signals. For example, the duty cycle is increased to increase the $T_{ON}$ duration and reduced to decrease the $T_{ON}$ duration. The period of the PWM signals is configured to match that of the signal applied to the capacitors **302***a*, **302***b* (Va, Vb). Thus, for example, for a 6.78 MHz signal applied to the capacitors **302***a*, **302***b*, the period of the PWM signals would be approximately 147.5 ns. The gate drivers **708***a*, **708***b* amplify the PWM signals as applicable to operate the switches **304***a*, **304***b*.

**[0082]** As described in reference to control circuitry **306** of FIG. **3**, the control circuitry **706** controls the ZVS of the switches **304***a*, **304***b* and the effective capacitance of the capacitors **302***a*, **302***b* by controlling the shorting duration $T_{ON}$. In addition, the control circuitry **706** adjusts the ZVS timing for turning the switches **304***a*, **304***b* ON to account for switching control delays. For example, electronic circuitry has some inherent signal processing and propagation delays, which become more readily apparent when circuits are operated at higher frequencies because delay times represent greater portions of operating signal periods. The control circuitry **706** can monitor such delays and adjust the ZVS timing for the switches **304***a*, **304***b* accordingly.

**[0083]** The comparators **710***a*, **710***b* are used to monitor the control signals applied to the switches **304***a*, **304***b*. More specifically, when transistors (e.g., MOSFETs) are used for the switches **304***a*, **304***b*, the comparators **710***a*, **710***b* can be configured to monitor for a voltage slightly below the threshold voltage, for example, the threshold voltage less a voltage offset (δ) ($V_{th}$—δ). The magnitude of the voltage offset (δ) is less than the magnitude of the threshold voltage ($V_{th}$) of the associated transistor.

**[0084]** For example, as shown in FIG. **7**, the non-inverting ("+") input terminal of each comparator **710***a*, **710***b* is electrically connected to the control terminal (e.g., gate) of its respective switch **304***a*, **304***b*. The inverting ("−") input terminal of each comparator **710***a*, **710***b* is electrically connected to a reference voltage $V_1$ or $V_2$ for the respective switch **304***a*, **304***b*. The reference voltages, $V_1$ and $V_2$, can be set at the threshold voltage ($V_{th}$) of the associated switch **304***a*, **304***b* or the threshold voltage less a voltage offset ($V_{th}$−δ). In this configuration, each comparator **710***a*, **710***b* will output a high signal value when the voltage of the gate drive signal for its respective switch **304***a*, **304***b* exceeds the applicable reference voltage $V_1$ or $V_2$, thereby, indicating that the respective switch **304***a*, **304***b* is ON.

**[0085]** As illustrated in FIG. **7**, the control circuitry **706** is symmetric, so, for simplicity, the control circuitry will be described in the context of controlling only one of the switch/capacitor pairs (switch **304**/capacitor **302***a*). The counter **704***a* and controller **702** control the ZVS timing for the switch **304***a*. The counter **704***a* receives timing input signals from both comparator **308***a* and comparator **710***a*. As described above, the output signal of comparator **308***a* indicates when the voltage across the capacitor **302***a* (Va) crosses zero, and the output signal of comparator **710***a* indicates when the switch **304***a* turns ON. The counter **704***a* measures the delay in turning the switch **304***a* ON ("switching delay") by measuring the timing difference between the output signals of comparator **308***a* and comparator **704***a*. For example, the counter **704***a* can initiate a timer when an appropriate edge (rising or falling) of the output signal from comparator **308***a* is received, and stop the timer when the output signal of comparator **710***a* indicates that sufficient drive voltage is being applied to switch **304***a* to turn switch **304***a* ON.

**[0086]** The measured switching delay is provided to the controller **702**. The controller **702** provides control signals to the PWM generator **707** to shift the phase of the PWM signal sent to gate driver **708***a* in order to decrease the switching delay for switch **304***a*. For example, the phase of the PWM signal sent to gate driver **708***a* can be advanced by an amount equivalent to the measured switching delay. In some examples, the controller **702** can monitor the switching delay each time the switch **304***a* is turned ON, and make adjustments to the PWM signal as appropriate. In some examples, the controller **702** can adjust the PWM signal until the switching delay is minimized. That is, the controller **702** can adjust the PWM signal until the switching delay is zero or approximately zero within the limitations of the circuit components (e.g., within the precision of the counters **704***a*, **704***b*).

**[0087]** FIG. **8** depicts the dynamically tunable capacitor circuit **800** with an example of a third implementation of the control circuitry **806**. The control circuitry **806** includes a controller **802**, phase detection circuits **804***a*, **804***b*, integrator circuits **805***a*, **805***b*, comparators **807***a*, **807***b*, flip-flops **809***a*, **809***b*, and gate drivers **808***a*, **808***b*. The tunable capacitor circuit **800** is similar to that described in reference to FIG. **3**, and includes voltage divider circuits **812***a*, **812***b* and an additional set of comparators **810***a*, **810***b*.

**[0088]** The controller **802** can be, for example, a microcontroller, a computer processor, an FPGA, or an ASIC. The controller **802** can include or be coupled to a computer readable storage device such as, for example, random access memory, flash memory, or other appropriate memory device. In some examples, the controller **802** can be a PWM generator.

**[0089]** As described in reference to control circuitry **306** of FIG. **3**, the control circuitry **806** controls the ZVS of the switches **304***a*, **304***b* and the effective capacitance of the capacitors **302***a*, **302***b* by controlling the shorting duration $T_{ON}$. In addition, the control circuitry **806** adjusts the ZVS timing for turning the switches **304***a*, **304***b* ON to account for switching control delays. For example, electronic circuitry typically has at least some inherent signal processing and propagation delays, which become more readily apparent when circuits are operated at higher frequencies because delay times represent greater portions of operating signal periods. The control circuitry **806** can monitor such delays and adjust the ZVS timing for the switches **304***a*, **304***b* accordingly.

**[0090]** The comparators **810***a*, **810***b* monitor the control signals applied to the switches **304***a*, **304***b*. More specifically, when transistors (e.g., MOSFETs) are used for the switches **304***a*, **304***b*, the comparators **810***a*, **810***b* detect when the gate drive signals meet the threshold voltage ($V_{th}$) of the associated transistor. In some examples, the comparators **810***a*, **810***b* monitor for a voltage slightly below the